

(SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2026	(Semester)	2	(Course No.)	2150418101
(Class)	01	(Open to)	3 IT (),	(Course Classification)	-IT / -
/	3.0 (1) / 3		100	가	가
(Office)	051306	(Telephone)	02-820-0710	(e-mail)	chlee@ssu.ac.kr
	(FL), (PBL)				
	(*) (ABEEK Classification)			(*) (ABEEK Requirement)	
	(C),				
(Course Description)	Top-down , HDL , Counter, Shifter Subsystem				

Verilog HDL	
	IT

가	(100)	(100%)
	100	100

(Required Texts)		* /Digital System Designs and Practices////Ming-Bo Lin/Wiley/2008/
		* /Modeling, synthesis, and rapid prototyping with the Verilog HDL/M Ciletti/Prentice-Hall/1999/
	()	* /HDL SOC IP / / /2004/
		* / LMS/2024
	(C)	
	Engaged learning	
	: / 40%, 15%, 35%, 10%	

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2.

(Week)	(Keyword)	(Description)		(Texts)
01	, HDL	HDL , Verilog		,
02	Verilog HDL	VerilogHDL syntax.	,	,
03	Dataflow	,	,	,
04	Simulation	Verilog HDL S/W , simulation , Testbench	, , , ,	,
05	Behavioral	Behavioral H/W	,	,
06		: FIR filter .		, ()
07	Behavioral	Behavioral H/W (assignment),	, ,	,
08	Behavioral	Behavioral (selection loop),	,	,
09	FSM	Finite state machine - state diagram, :	,	, ()
10	FSM	Finite state machine – model and state reduction,	,	,
11	FSM	Finite state machine - ASM chart, :	, ,	,
12	, task,	Verilog HDL system task . :	, , , , , ,	,
13	Design example	Design example: Combinational logic, :	, , , , , , ,	,
14	Design example	Design example: sequential logic,	, ,	,
15	,	: FIR filter, () /	, , ,	11/22() 1:00 – 3:30: ()

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3. ()

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	Open-ended problem		
	Teamwork		
	Communication skills		